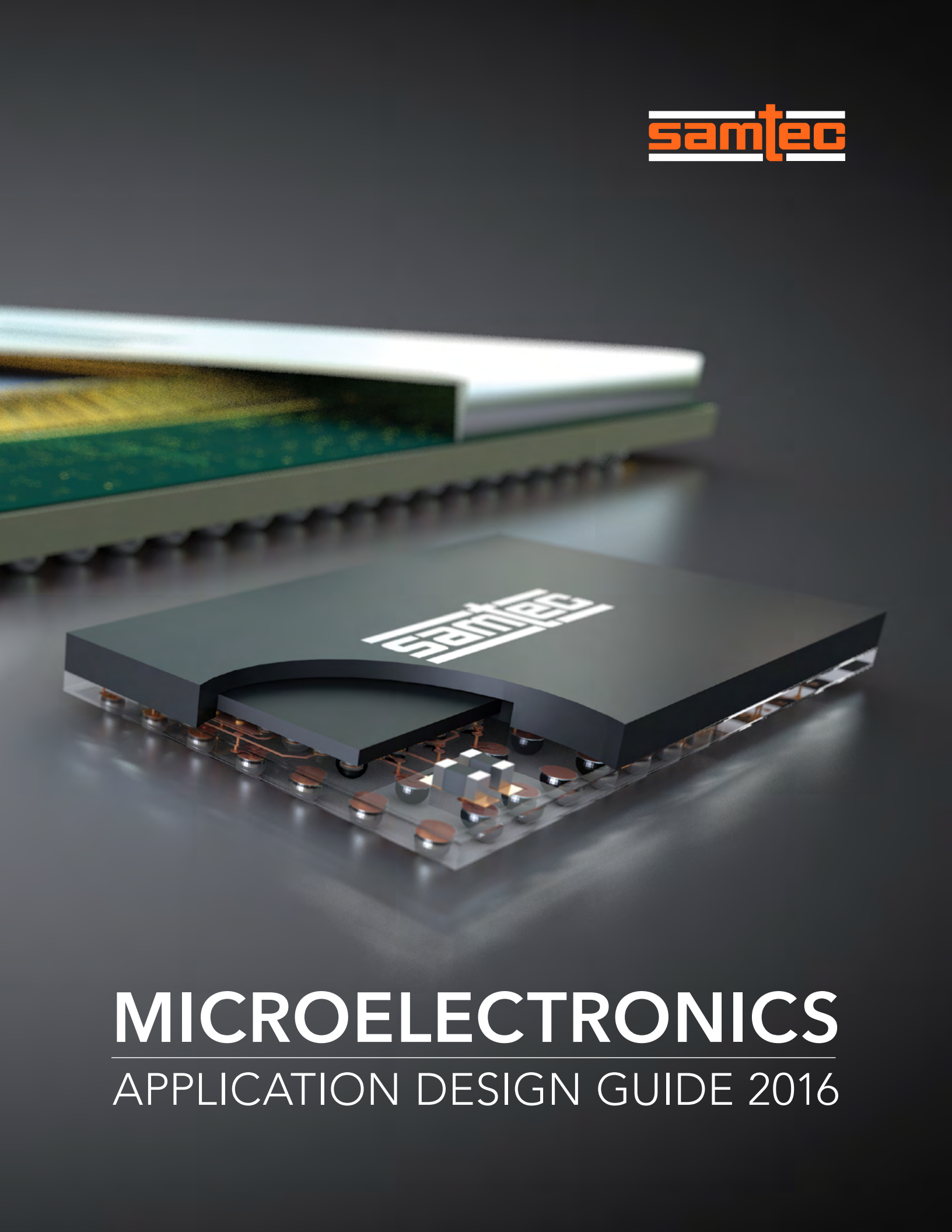


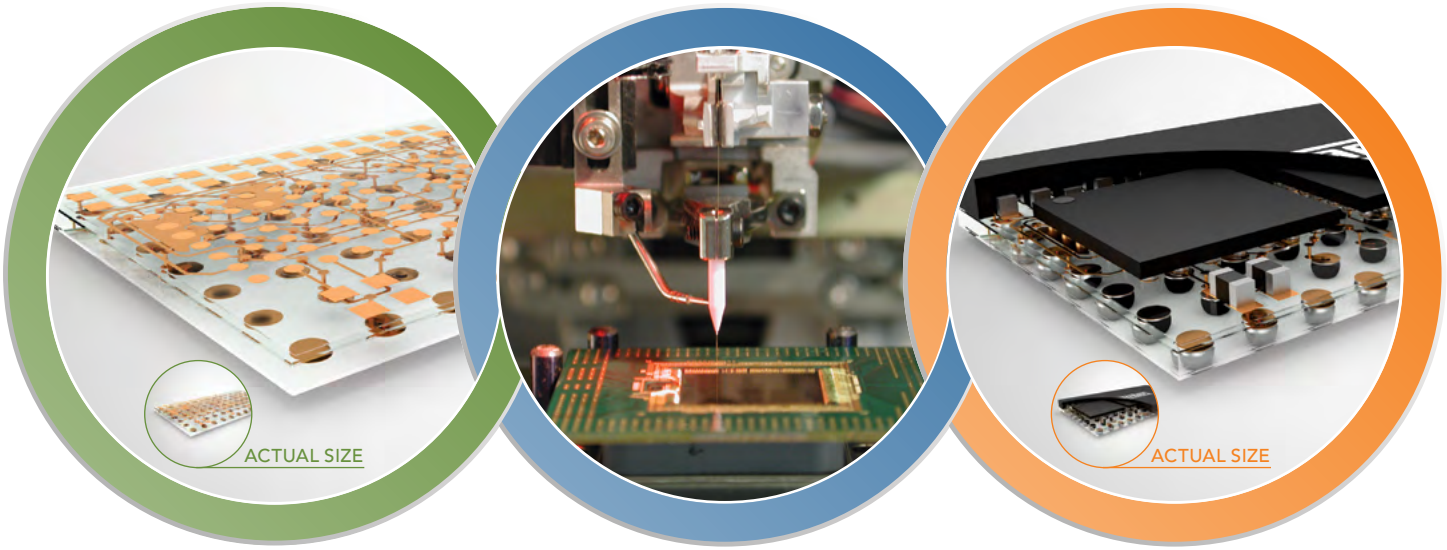
MICROELECTRONICS

APPLICATION DESIGN GUIDE 2016

NEXT GENERATION MICROELECTRONICS SOLUTIONS

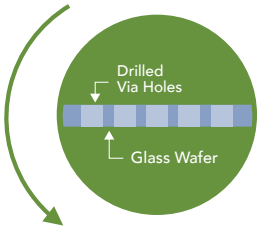
INNOVATION + MINIATURIZATION = STREAMLINED SIGNAL PATH

Samtec leverages industry-leading expertise in high-speed interconnect design, system level signal integrity, and advanced IC packaging, to develop innovative advanced microelectronics solutions that are optimized for performance, size and cost, to support next generation systems, modules and components.



MICROELECTRONICS CAPABILITIES TAILORED TO YOUR APPLICATION

Choose any level of technology or combination of technologies to build your solution.

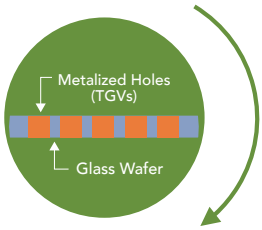


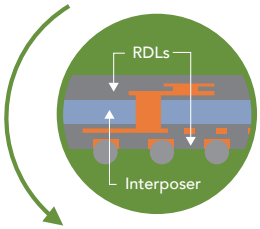
GLASS CORE TECHNOLOGY - LEVEL 1

High-density via holes are drilled into high quality glass wafers

GLASS CORE TECHNOLOGY - LEVEL 2

Via holes are filled & hermetically sealed to create the Through-Glass Vias (TGVs)



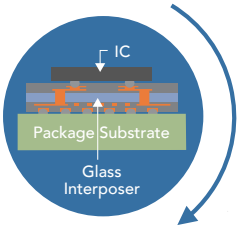


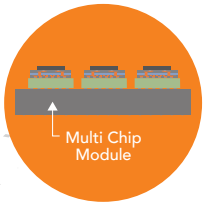
GLASS CORE TECHNOLOGY - LEVEL 3

Circuits are formed by applying Redistribution Layers (RDLs) to the TGVs

IC PACKAGING & ASSEMBLY

Die attach, flip chip, wirebond & finishing for high-performance IC packages

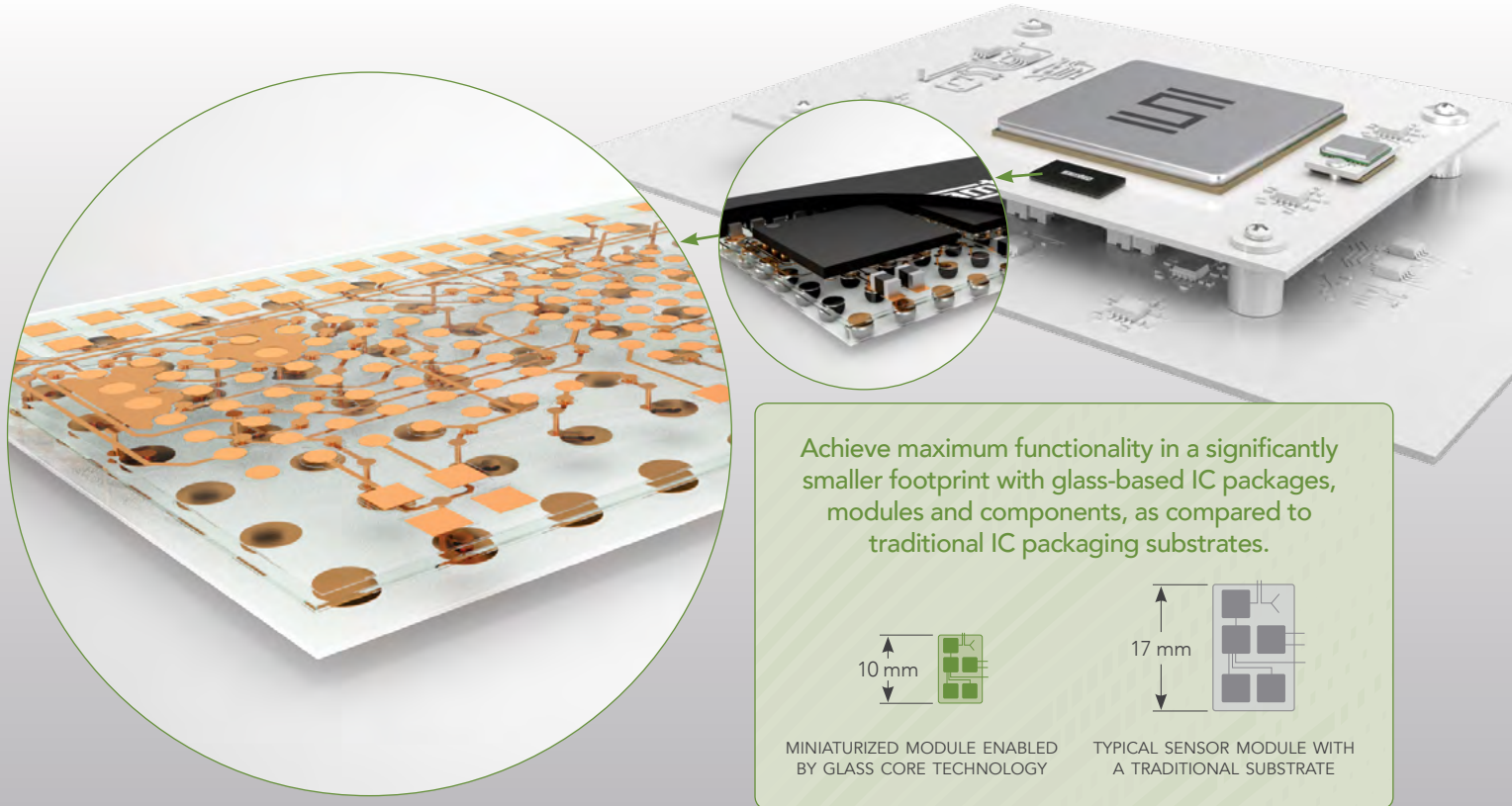




SYSTEM LEVEL SOLUTIONS

Integration of IC packages to create MCMs and other high-performance components

GLASS CORE TECHNOLOGY
EXTREME IC PACKAGE MINIATURIZATION



Achieve maximum functionality in a significantly smaller footprint with glass-based IC packages, modules and components, as compared to traditional IC packaging substrates.

MINIATURIZED MODULE ENABLED BY GLASS CORE TECHNOLOGY

TYPICAL SENSOR MODULE WITH A TRADITIONAL SUBSTRATE

GLASS PACKAGE SUBSTRATES | SUPERIOR PROPERTIES = EXTREME MINIATURIZATION

Glass is an excellent low loss, lower cost solution compared to traditional silicon and organic substrates, and provides a solid processing infrastructure for IC packaging applications. Additional benefits of glass substrates include:

- Electrical conductivity
- TCE match to the glass
- Increased reliability of large I/O dies with fine pitches
- Low warp
- Hermetic Cu-based vias
- Reduced wafer breakage
- Thermal cycling reliability
- Improved thermal conductivity vias for logic, power or other applications where thermal management is critical
- Biomedical sensors can be assembled by wafer level processing
- Excellent packaging platform for incorporating optical waveguides, turning mirrors

Samtec's Glass Core Technology (GCT) allows for IC packaging solutions with faster cycle times and KGD testing at higher packaging integration levels, at the lowest cost in the marketplace.

DESIRED PROPERTIES		GLASS	SILICON	ORGANIC LAMINATE
TTV	< 5 µm			
Warp	< 2 µm / 20 mm			
Insulation Resistance	High			
Optical Transparency	Optical I/O			
Surface Roughness	< 5 nm			
TCE	3.2 ppm / C			
Hermetic Vias	Mil-Spec.			

GLASS CORE TECHNOLOGY PROCESS

Samtec's Glass Core Technology (GCT) is a proprietary process that leverages the performance benefits of glass by creating small diameter, fine pitch Through-Glass Vias (metalized and hermetically sealed), and the formation of circuits on glass via a unique thin-film Redistribution Layer process. The result is a performance optimized, ultra-miniaturized substrate, ideal for next generation IC packaging. See pages 12-13 for current Glass Core Technology Design Rules & Guidelines.

THROUGH-GLASS VIA (TGV) METALIZATION

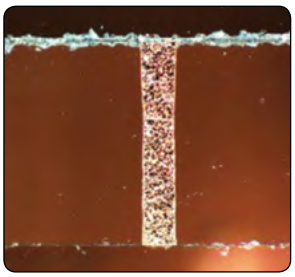
The challenges of generating small diameter through-holes in glass with fine pitches are eliminated with Samtec's proprietary Glass Core Technology process, which enables:

- Hermetic / high conductivity vias
- Miniaturization:
  - 100 µm (0.1 mm) pitch, with roadmap to 40 µm (0.04 mm)
  - 40 µm (0.04 mm) diameter, with roadmap to 10 µm (0.01 mm)
- Laser formed holes:
  - 200+ µm (0.2 mm) thick glass
  - Optimized coplanarity (< 20 µm wafer bow)

Samtec offers three types of TGVs: tapered, hourglass and straight. TGV type is dependent upon industry and application requirements.

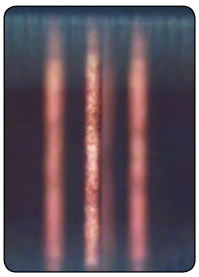
Contact **sme@samtec.com** to discuss your specific application and requirements.

Metalized Through-Glass Vias



Hourglass

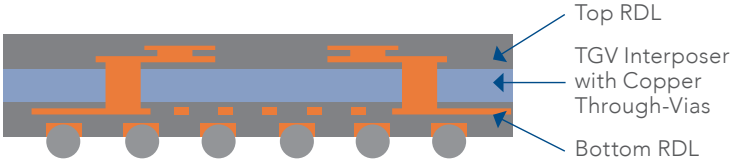
Tapered

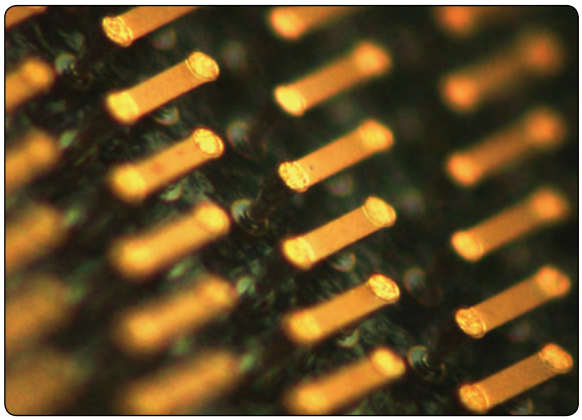


Straight

REDISTRIBUTION LAYER (RDL) CIRCUIT PATTERNING

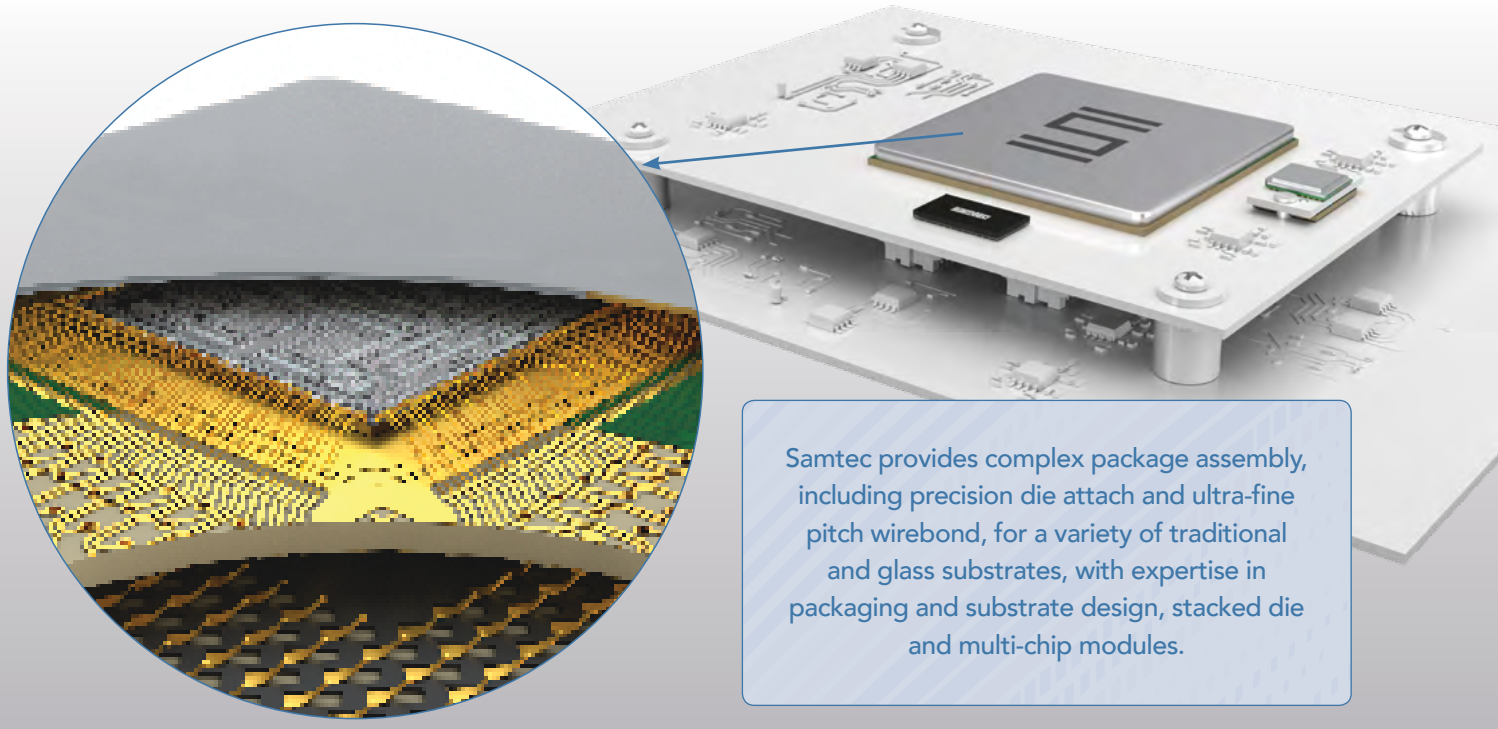
Samtec's Redistribution Layer (RDL) technology is a unique, thin-film approach to interfacing with the TGVs. This technique enables circuit formation on glass substrates which provides a low loss, fan-out of chip and package interconnects at a lower cost than silicon interposers.





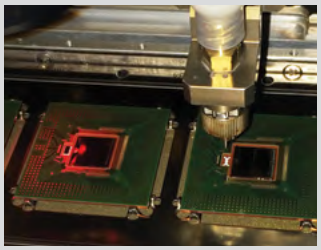
Through-Glass Via Interposer with Redistribution Layers

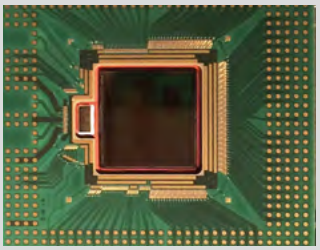
IC PACKAGING CAPABILITIES
DESIGN, ASSEMBLY & SUPPORT



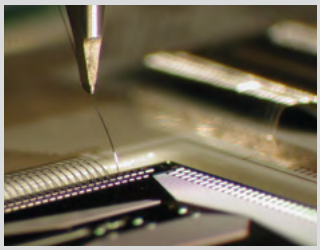
Samtec provides complex package assembly, including precision die attach and ultra-fine pitch wirebond, for a variety of traditional and glass substrates, with expertise in packaging and substrate design, stacked die and multi-chip modules.

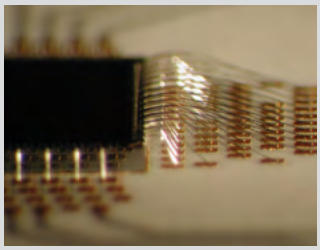
COMPLEX IC PACKAGING | DIE ATTACH • WIREBOND • FLIP CHIP • FINISHING



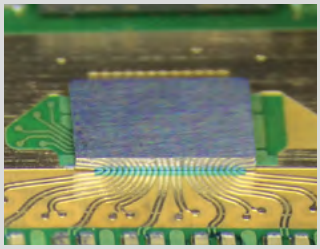


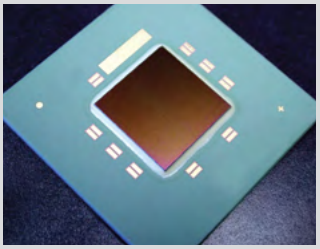
Precision Placement Die Attach



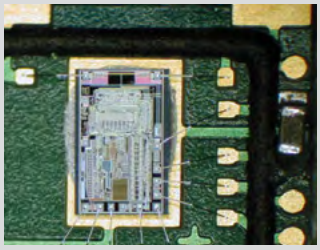


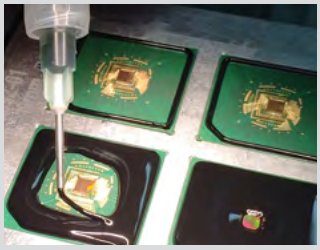
Fine Pitch & Low Profile Wirebond





Maximum Density Flip Chip & Underfill





Dam & Encapsulation

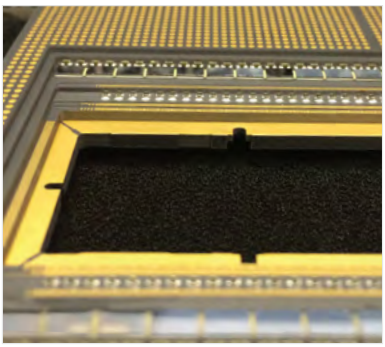
See pages 14-15 for current IC Packaging Design Rules & Guidelines. Contact SME@samtec.com to discuss your application.

ADVANCED MICROELECTRONICS APPLICATIONS

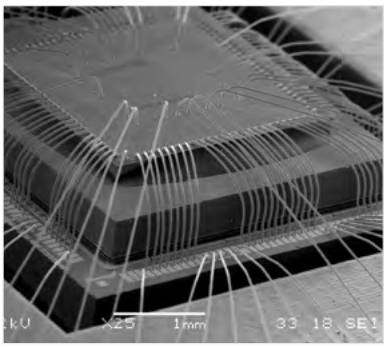
Samtec's Microelectronics Group and Teraspeed® Consulting Technology Centers provide unprecedented support for advanced microelectronics packaging design and simulation, from prototype to full-volume production, with analysis expertise that enables IC application optimization.

APPLICATION SPECIFIC DESIGN & SUPPORT

- Advanced design of OC-48, XAUI and OC-192 packages
- SI-enabled layouts for 28 Gbps and 56 Gbps systems
- Custom 2D and 3D applications
- MEMS, Microfluidic MEMS
- Image Silicon Photonics & Modules
- Smart Systems-on-Interposer
- Prototype assemblies and real-time testing
- Package characterization
- I/O buffer sizing & design kits



MCM with Flip Chip



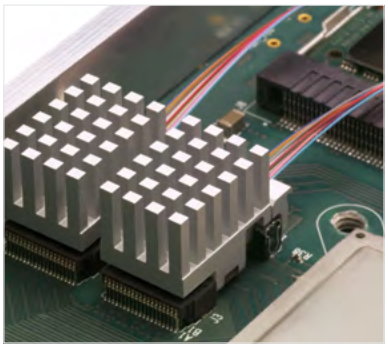
Custom 3D Packaging Applications

OPTICS & PHOTONICS

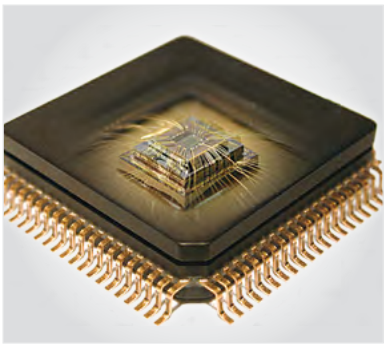
Samtec Optics and Microelectronics Groups work in collaboration to design and develop advanced solutions, such as our next generation SiPho Optical Engines.

- VCSEL-based micro optics
- Advanced PD & VCSEL Silicon Photonics
- Stacked interposers

Contact **sme@samtec.com** to discuss your application.



Optical Engine Design & Manufacturing

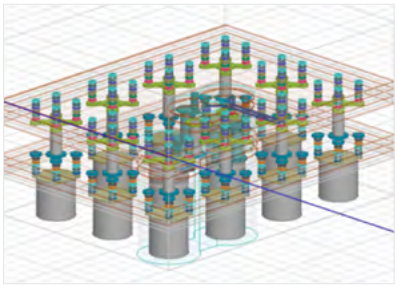


MEMS Assembly

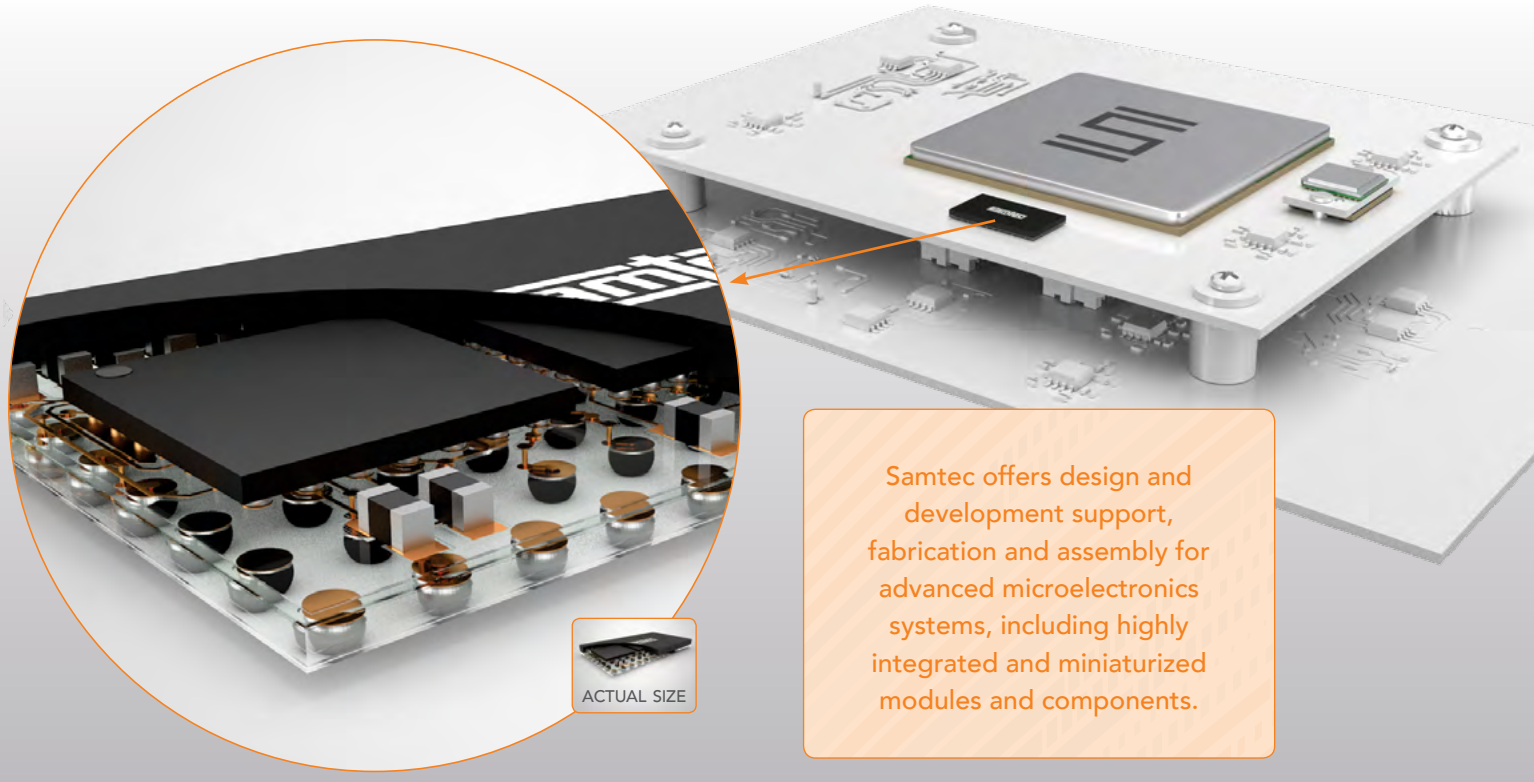
SUBSTRATE DESIGN, MODELING, TESTING & PROCUREMENT

Samtec also offers assistance in materials selection and procurement, as well as modeling, test and design services.

- Substrate design, including ceramic, flex, organic (FR4, BT, Rogers), silicon, metal, borosilicate glass, cover glass, sapphire, and fused silica, BGA and MCM design
- Layout software (e.g. SOLIDWORKS, PADS)
- Substrate modeling, including full wave EM (Electromagnetic) tools, data processing and channel simulation
- Procurement of substrates through approved vendors



SYSTEM LEVEL SOLUTIONS
DESIGN SUPPORT & FABRICATION

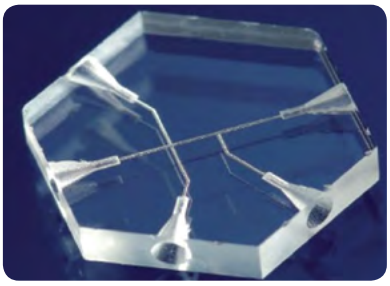


Samtec offers design and development support, fabrication and assembly for advanced microelectronics systems, including highly integrated and miniaturized modules and components.

GLASS CORE TECHNOLOGY | ENABLING INTEGRATION + MINIATURIZATION

Glass Core Technology-based substrates are ideal for a variety of industries & applications:

- Industrial tracking and data collection
- Orthopedic rehabilitation / recovery
- Animal health monitoring
- Medical external monitoring
- Fuel and power consumption
- Home security and infrared cameras
- Wearable technology
- Automotive monitoring & tracking

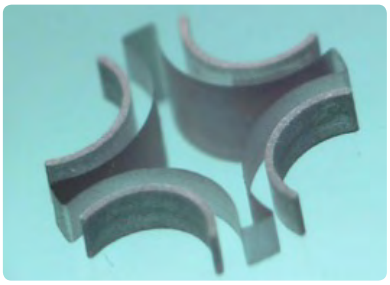


Microfluidic Channels

GCT enables endless possibilities for highly integrated, ultra-miniaturized modules and components, including:

- Incorporation of glass interposers for 2.5D and 3D solutions
- Integrated microfluidic channels in devices: laser formed holes and channels in glass, available in any construction with hermetically metalized vias
- Sapphire substrates with platinum vias and etched cavities for biocompatible solutions
- Miniaturized biomedical devices
- Active and passive components: RF filters, optics modules, VCOs, etc.

Contact the specialists at sme@samtec.com to discuss your application.



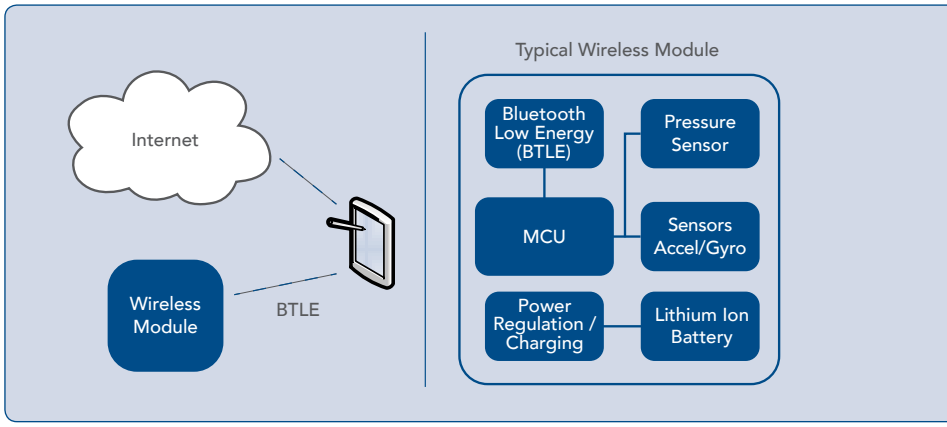
Holes Formed in Fused Silica

WIRELESS SMART MODULES: PROVIDING INTELLIGENCE TO THE MODULE

Surface mount modules enabled by Samtec's Glass Core Technology incorporate a controller, communication (radio), power management and sensor elements, while offering extremely low power consumption. Wireless Smart Modules can connect to existing or next generation sensors.

ENDLESS DESIGN POSSIBILITIES

- Smallest devices for sensor alerts
- Application-specific based designs
- "Plug-n-Play" solutions
- Expandable up to 256 bio/chem sensors
- Cloud-based sensor for data access



SMART MODULE ADVANTAGES

- Improved system performance:
  - Low loss / high frequency properties
  - Capable of high-density I/O, designed for high-speed / high frequency performance
  - Reduces external interconnects and overall weight, resulting in lower overall system cost
- Designed for high volume manufacturing; low cost solution
- Hermetic sealing for harsh environments
- Ultra miniaturized and integrated:
  - 3D system integration with ultra micro footprint and weight; ideal for microfluidic applications
  - Small feature size (<10 µm) allows for more capabilities in the same volume
  - Vias may be located anywhere as part of standard processing
  - Embedded passive and active components simplifies end user design

MINIATURIZED COMPONENTS & MODULES

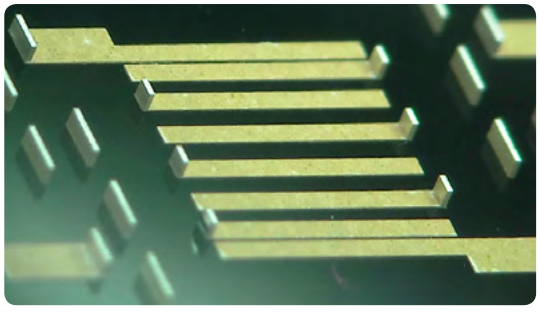
Samtec's Glass Core Technology is ideal for both active and passive devices.

PASSIVE DEVICES:

- Band, low, high pass filters
- Inductors, capacitors and resistors
- Couplers
- Splitters
- Delay lines
- Attenuators
- Antennas
- 50 ohm loads

ACTIVE DEVICES:

- VCOs
- Amplifiers
- Tunable filters
- Optics modules

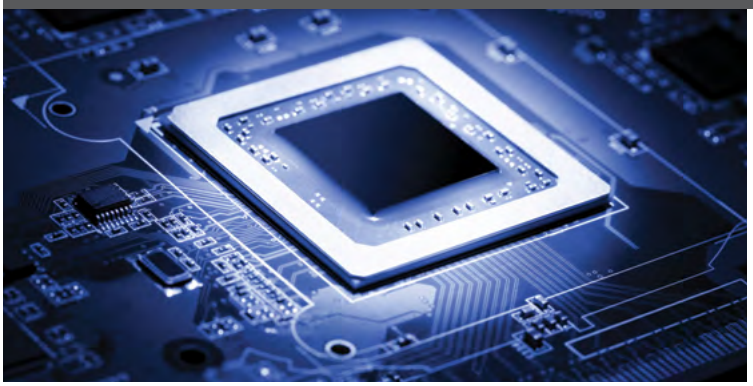


Glass Core Technology-based RF Filter

SAMTEC TECHNOLOGY CENTERS
INTEGRATION LEADS TO INNOVATION

Samtec Technology Centers are dedicated to developing and advancing technologies, strategies and products to optimize system performance and cost. These complimentary, cross-functional groups leverage their expertise and experience to ensure complete system optimization from Silicon-to-Silicon™.

SAMTEC MICROELECTRONICS GROUP



The Microelectronics Group brings a unique blend of signal integrity and advanced IC packaging expertise to provide full channel system support.

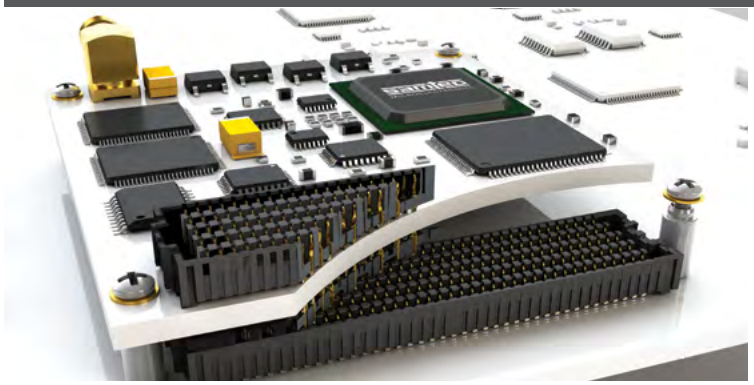
Capabilities include precision die attach, fine pitch and low profile wirebond, flip chip, underfill and stacked die, complete IC-to-Board design, support and manufacturing of IC packaging, glass and traditional substrates, and micro optical engines.

SIGNAL INTEGRITY GROUP

The Signal Integrity Group (SIG) provides in-house signal integrity expertise for complex applications, with live EE support available 24/7 worldwide.

Services include full-channel analysis, high-data rate simulations, application-specific design and development assistance, and advanced design support.

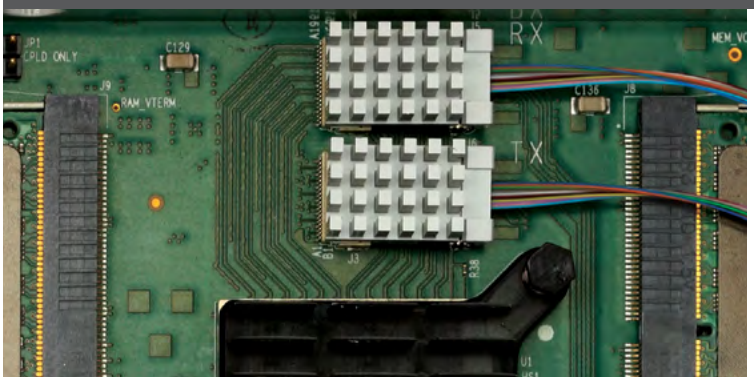
ADVANCED INTERCONNECT DESIGN



The Samtec Advanced Interconnect Design Technology Center (AID) ensures your interconnect systems are designed for quality, design flexibility, ease-of-processing, and even supply chain risk minimization.

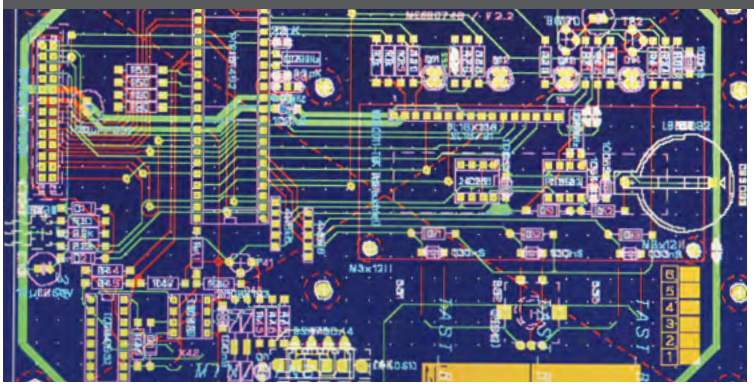
The AID Tech Center provides precision stamping, plating, molding and automated assembly for high-speed, fine pitch, array, and micro-rugged interconnects.

SAMTEC OPTICAL GROUP



The Samtec Optical Group is an engineering team dedicated to the design, development, and application support of high-performance micro optical engines, active optical assemblies, and high-density ganged passive optical panel solutions.

TERASPEED® CONSULTING



Teraspeed® Consulting offers Tier 1 level signal integrity expertise and capabilities delivered directly to your engineering team.

Capabilities include complete system design, full channel signal and power integrity analysis and modeling, thermal management, in-depth signal integrity training, and signal integrity optimized advanced IC packaging for 28 Gbps and beyond.

HIGH-SPEED CABLE PLANT

The High-Speed Cable Technology Center focuses on R&D and manufacturing of precision extruded micro coax and twinax cable used for high-speed, high-density cable assemblies, including 26-38 AWG, 50/75/85/100 Ω impedance, and systems rated at 28 Gbps and beyond.

DESIGN GUIDELINES | GLASS CORE TECHNOLOGY

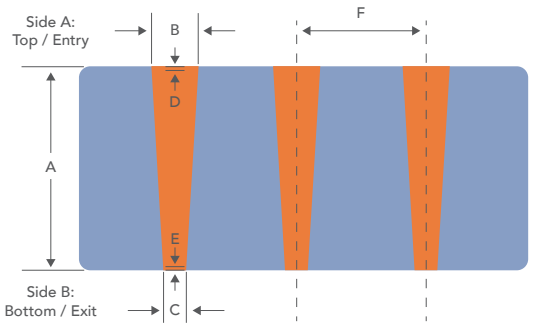
The following dimensions are guidelines designed to help release product to manufacturing as quickly as possible. Full capabilities are not limited to the specifications included in this document. Please contact SME@samtec.com for applications with tighter requirements.

THROUGH-GLASS VIA WAFERS & INTERPOSERS

Samtec Through-Glass Vias enable Through-Glass Via wafers and interposer die. TGV wafers permit the integration of glass and metal into a single wafer, while interposer die permit more efficient connections and cycle times.

The hermetically sealed wafers are manufactured from both high quality borosilicate and quartz glass. Through the use of high quality wafer material, combined with top metalization technology, Samtec wafers become a one of a kind packaging product.

THROUGH-GLASS VIA CROSS-SECTION VIEW



INTERPOSER DIE SPECIFICATIONS (FUSED SILICA)

DETAIL	UNITS (µm)
Nominal Thickness	500
TTV (Total Thickness Variation)	5
Top Via Diameter	70 ±5
Bottom Via Diameter	65 ±5
Via Pitch	150
Slots Width	70 ±5
Slots Length (Demonstrated)	1000

STANDARD TGV DESIGN GUIDELINES (BOROSILICATE GLASS)

	DETAIL	UNITS (µm)		
A	Nominal Glass Thickness*	200	300	500
	TTV (Total Thickness Variation)	5		
B	Side A Via Diameter	40 ±5	60 ±5	70 ±5
C	Side B Via Diameter	40 ±5	60 ±5	70 ±5
D	Side A Via Depth	< 0.5		
E	Side B Via Depth	< 0.5		
F	Via Pitch	2x B		
	Via Positional Accuracy	±13		

*Custom nominal thicknesses also available.

WAFER SPECIFICATIONS (BOROSILICATE GLASS)

DETAIL	UNITS (µm)		
Nominal Thickness*	200	300	500
TTV (Total Thickness Variation)	5		
Top Via Diameter	80 ±5	85 ±5	100 ±5
Bottom Via Diameter	50 ±5		
Via Pitch	120	160	200

*Custom nominal thicknesses also available.

FUSED SILICA

Characteristics:

- High purity glass
- Wide operating temperature range
- High thermal shock resistance
- Low coefficient of thermal expansion
- Low fluorescence

Applications:

- Bio / Medical
- Photonics
- Biometric Sensors

BOROSILICATE

Characteristics:

- Excellent clarity and rigidness
- High thermal shock resistance
- Low density glass
- Low thermal expansion
- Spectral transmittance cof. 90%

Applications:

- Bio / Medical
- 2.5D / 3D Packaging
- Display / Photonics
- RF MEMS
- Optoelectronics

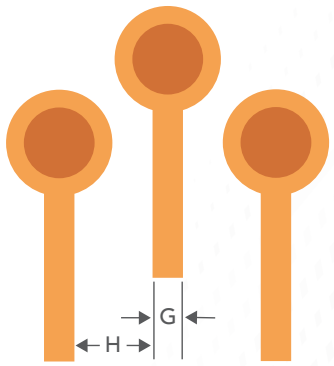
REDISTRIBUTION LAYER (RDL)

Redistribution Layer (RDL) technology provides a unique thin-film approach for interfacing to TGVs. The technique enables circuit formation on various glass substrates.

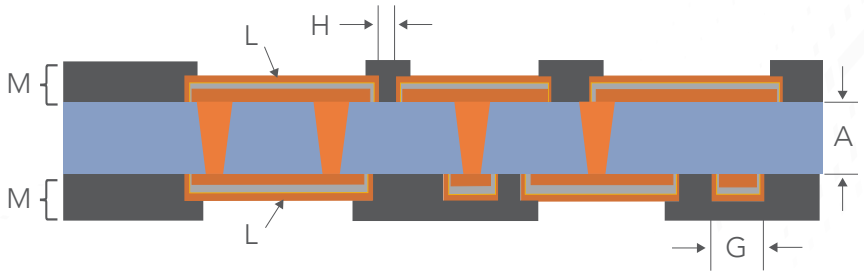
GLASS CORE TECHNOLOGY CAPABILITIES

	SPECIFICATIONS	CURRENT	ROADMAP
	No. of Metal Layers per Side	2	4
A	Glass Core Thickness	300 to 700 µm	100 µm
	Core Via Diameter	40 µm	10 µm
	Core Via Pitch	100 µm	40 µm
G, H	Line / Spacing	15 µm / 15 µm	5 µm / 5 µm
L	Copper Thickness	1-10 µm	
M	Polyimide Thickness 1 & 2	5 µm	
	Solder Ball Types	Sn63Pb37, PbSn5, PbSn10, SAC	Cn / Sn Pillars
	Under Bump Metalization (UBM)	ENIG	

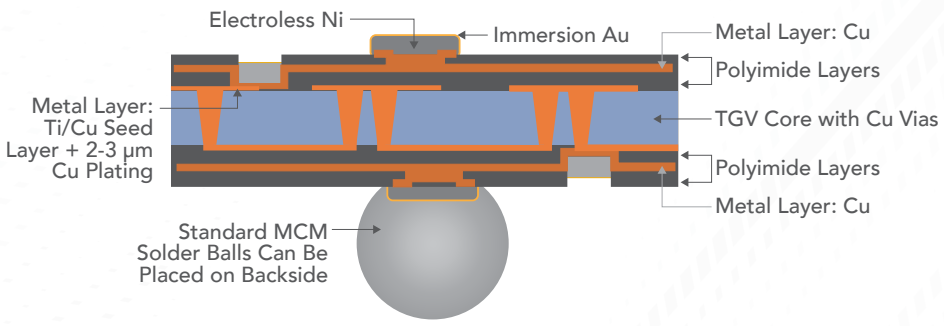
TOP VIEW OF CIRCUIT FOR TOP / BOTTOM RDL



CROSS SECTION - 2 METAL LAYERS (CURRENT CAPABILITY)



CROSS SECTION - 4 METAL LAYERS (FUTURE CAPABILITY)



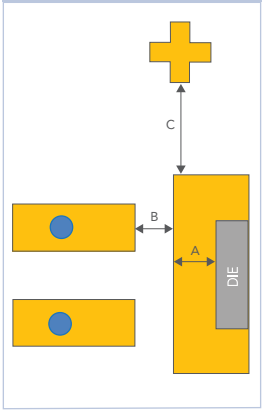
DESIGN GUIDELINES | IC PACKAGING & ASSEMBLY

The following dimensions are guidelines designed to help release product to manufacturing as quickly as possible. Full capabilities are not limited to the specifications included in this document. Please contact SME@samtec.com for applications with tighter requirements.

DIE ATTACH

- Minimum distance between surrounding square of fiducial and neighboring objects must be 0.048 mm
- Gray level contrast between background and fiducial must be a minimum of 100 gray levels out of 256
- Background of fiducial must not have a structure and background must be single-colored gray level
- Maximum die size for dipping: 50 mm x 50 mm
- No waffle-pack handling for die < 1 mm^2
- Maximum length to width ratio for components: 5:1
- Saw kerfs must be at least 25 µm and into the dicing tape (through the entire wafer thickness)
- Die attach materials can be non-conductive, conductive, die-attach-films (DAF) and solder preforms; other processes can be discussed per customer requirements

TOP DOWN



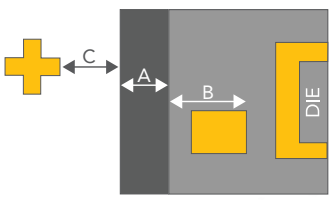
DIE ATTACH REQUIREMENTS (TYPICAL)

	DESCRIPTION	ORGANIC (min)	CERAMIC (min)
	Minimum Die Size	0.010" (250 µm)	0.010" (250 µm)
A	Overlap of Die Attach Ground Plane to Die Edge	0.020" (500 µm)	0.020" (500 µm)
B	Space Between Die Attach Ground Plane to Wirebond Pad	0.020" (500 µm)	0.020" (500 µm)
C	Space Between Fiducial Edge to Die Attach Ground Plane Edge	0.010" (250 µm)	0.006" (150 µm)

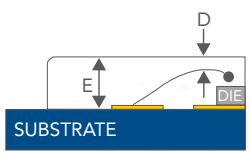
DAM & ENCAPSULATE

- Maximum encapsulation thickness (board surface to top of encapsulation): 0.024" (600)
- Automated dispense tool heated work area: 12" x 16"
- Total work area: 20" x 30"
- Machine positioning accuracy and repeatability: +/- 0.001"

TOP DOWN



SIDE PROFILE



TYPICAL PACKAGE DESIGN RULES

	DESCRIPTION	ORGANIC (min) INCHES (µm)
A	Dam Width	0.012" (300)
B	Space of Dam to Wirebond Lead Edge	0.012" (300)
C	Space of Fiducial to Dam*	0.007" (175)
D	Overlap of Encapsulation to Top of Wirebond Loop	0.007" (175)
E	Height of Encapsulation**	= A / 2

*Must be outside encapsulated region
**Board surface to top of encapsulation

FLIP CHIP & UNDERFILL

Package Size (approximate):

- Min: 10 mm x 10 mm
- Max: 63 mm x 63 mm

Flux:

- Tac-Flux-025 & WS-609
- Other no-clean flux types
- Water soluble flux types

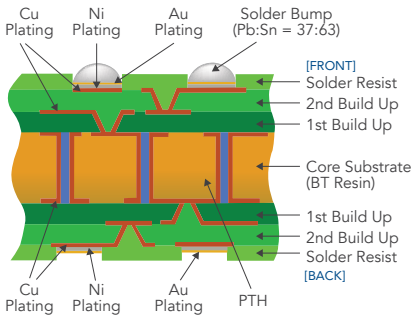
Substrate BGA Solder Ball:

- Min Size: 0.18" dia. (approx.)
- Max Size: 0.025" dia. (approx.)
- Material: Eutectic Pb:Sn (37:63) or Pb-Free

Substrate BGA Pad:

- Closest Pitch: 0.80 mm x 0.80 mm
- Furthest Pitch: No constraint
- Pad Layout: Any configuration is acceptable

SUBSTRATE STRUCTURE (TYPICAL)

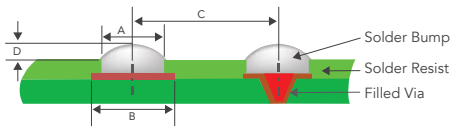


LAYER THICKNESS (TYPICAL)

LOCATION	STANDARD (µm)	CUSTOM (µm)
Core Substrate	800	400*
Core Cu	25	21
Build-up Cu	14.5	2
Insulation Layer	33	12
Solder Resist Layer	21	18
Nickel Plating	3 - 7	
Gold Plating	0.03 ~ 0.12	

No. of Build Up Layers: 1, 2, 3, 4 / side;
No. of Core Layers: 2, 4; *Coreless also available

FLIP CHIP PAD DESIGN RULE



LAYER THICKNESS (TYPICAL)

	ITEM	STANDARD	CUSTOM
A	Flip Chip Pad Diameter (Solder Resist Opening)	100 µm	75 µm
B	Flip Chip Pad Metal Land Dia.	145 µm	100 µm
C	Flip Chip Pad Pitch	225 µm	130 µm
D	Solder Bump Height	32 µm ± 5 µm	

WIREBOND

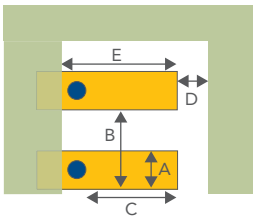
Plating and layout requirements for substrate pad design as well as wire parameters:

- Wedge Bond - ENIG plating is acceptable; typical wire types include Al, Au and Pt
- Ball Bond - ENEPIG plating is recommended; typical wire types include Au and Cu

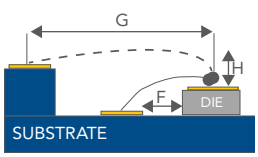
Processes that use Au ball bond, require Gold plate per MIL-G–45204, Type III, Grade A, Class 1:

- 99.9% purity minimum
- < 90 Knoop hardness
- 50 µ" thick, minimum

TOP DOWN

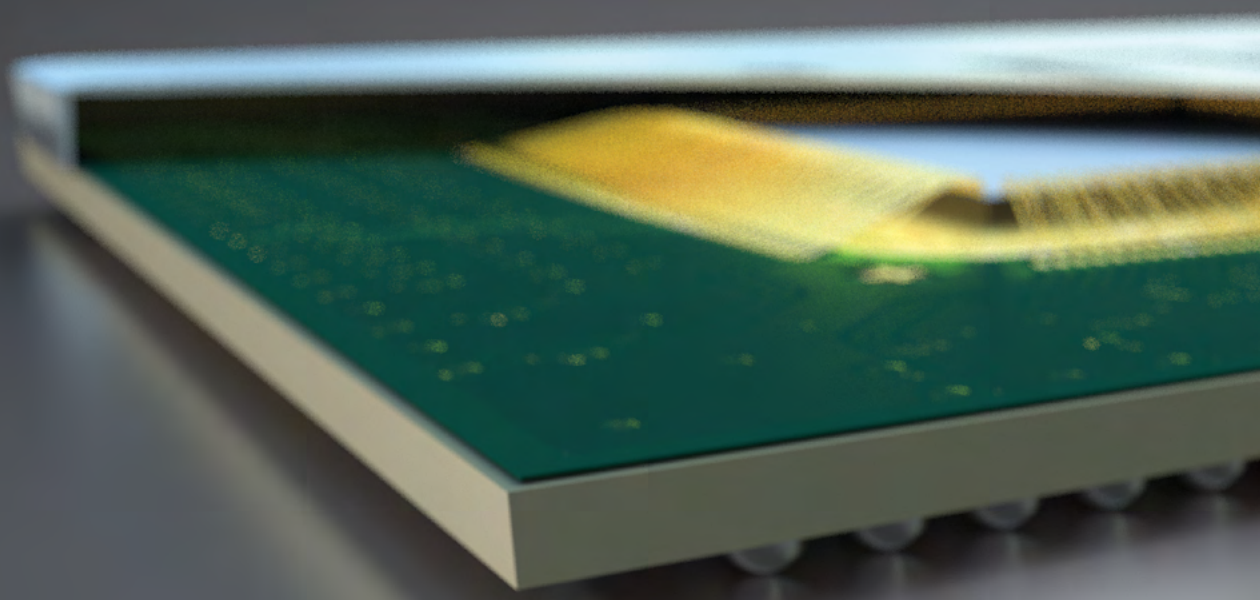


SIDE PROFILE



TYPICAL WIREBOND SPECIFICATIONS

	DESCRIPTION	ORGANIC (min)	CERAMIC (min)
A	Wirebond Pad	0.004" (100 µm)	0.003" (75 µm)
B	Wirebond Pad Pitch	0.008" (200 µm)	0.006" (150 µm)
C	Overlap of Wirebond Lead Edge to Via	0.008" (200 µm)	0.007" (175 µm)
D	Space Solder Mask to Wirebond Lead Edge	0.004" (100 µm)	-
E	Overlap of Wirebond Lead Edge to Solder Mask	0.008" (200 µm)	-
F	Space of Die Edge to Wirebond Lead Edge (assumes no ground plane for die attach)	0.015" (375 µm) or 2x Die Thickness (whichever is greater)	
G	Maximum Wire Length	0.250" (6350 µm)	
H	Maximum Wire Height	0.100" (2540 µm)	



samtec

SUDDEN SERVICE®

UNITED STATES • NORTHERN CALIFORNIA • SOUTHERN CALIFORNIA • SOUTH AMERICA • UNITED KINGDOM • GERMANY • FRANCE • ITALY • NORDIC/BALTIC
BENELUX • ISRAEL • INDIA • AUSTRALIA / NEW ZEALAND • SINGAPORE • JAPAN • SHANGHAI • SHENZHEN • TAIWAN • HONG KONG • KOREA

OCTOBER 2016